



Atty. Dkt. No. 035905-0118

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Igor G. KOUZNETSOV et al.

Title: TWO MASK FLOATING GATE EEPROM AND METHOD OF MAKING

Appl. No.: 10/066,376

Filing Date: 02/05/2002

Examiner: Unassigned

Art Unit: 2823

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**INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.56**

Commissioner for Patents
Washington, D.C. 20231

Sir:

Submitted herewith on Form PTO/SB/08 is a listing of documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR §1.56. A copy of each listed document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(b), before the mailing date of the first Office Action on the merits.

RELEVANCE OF EACH DOCUMENT

An English translation of the foreign-language documents is not readily available. However, the absence of such translation does not relieve the PTO from its duty to consider the submitted foreign language documents (37 CFR §1.98 and MPEP §609).

Applicants respectfully request that any listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 CFR §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

Respectfully submitted,

Date 6/13/02

By Leon Radomsky

Leon Radomsky
Attorney for Applicant
Registration No. 43,445

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Customer Number: 22428



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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

Date Submitted: June 13, 2002

(use as many sheets as necessary)

Complete if Known

Application Number	10/066,376
Filing Date	02/5/2002
First Named Inventor	Igor KOUZNETSOV et al.
Group Art Unit	2821
Examiner Name	Unassigned

Sheet

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of

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Attorney Docket Number 035905-0118

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	B1	4,500,905		Shibata		
	B2	6,185,122		Johnson et al.		
	B3	3,414,892		McCormack et al.	12/13/1968	
	B4	3,432,827		Sarno	3/11/1969	
	B5	4,535,424		Reid		
	B6	4,630,096		Drye		
	B7	4,672,577		Hirose		
	B8	4,710,798		Marcantonio		
	B9	4,811,082		Jacobs		
	B10	5,001,539		Inoue et al.		
	B11	5,089,862		Warner, Jr. et al.		
	B12	5,160,987		Pricer et al.		
	B13	5,191,405		Tomita et al.		
	B14	5,202,754		Bertin et al.		
	B15	5,266,912		Kledzik		
	B16	5,283,468		Kondo et al.		
	B17	5,398,200		Mazure et al.		
	B18	5,422,435		Takiar et al.		
	B19	5,426,566		Beilstein, Jr.		
	B20	5,434,745		Shokrgozar et al.		
	B21	5,453,952		Okudaira		
	B22	5,455,455		Kurtz et al.		
	B23	5,468,997		Imai et al.		
	B24	5,471,090		Deutsch		
	B25	5,481,133		Hsu		
	B26	5,495,398		Takiar et al.		
	B27	5,502,289		Takiar et al.		
	B28	5,523,622		Harada et al.		
	B29	5,523,628		Williams et al.		
	B30	5,552,963		Burns		
	B31	5,561,622		Bertin et al.		
	B32	5,581,498		Ludwig et al.		
	B33	5,585,675		Knopf		
	B34	6,612,570		Eide et al.		
	B35	5,654,220		Leedy		
	B36	5,693,552		Hsu		
	B37	5,696,031		Wark		
	B38	5,703,747		Voldman et al.		
	B39	5,780,925		Cipolla et al.		
	B40	5,781,031		Bertin et al.		
	B41	5,801,437		Burns		
	B42	5,915,167		Leedy		

Examiner Signature	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT
Date Submitted: June 13, 2002
(use as many sheets as necessary)

Sheet		2 of 7		Complete if Known	
				Application Number	10/066,376
				Filing Date	02/5/2002
				First Named Inventor	Igor KOUZNETSOV et al.
				Group Art Unit	2821
				Examiner Name	Unassigned
				Attorney Docket Number	035905-0118

U.S. PATENT DOCUMENTS					
B43	5,969,380		Syyedy		
B44	5,976,953		Zavracky et al.		
B45	5,985,693		Leedy		
B46	6,057,598		Payne et al.		
B47	6,072,234		Camien et al.		
B48	6,087,722		Lee et al.		
B49	6,133,640		Leedy		
B50	6,351,028		Akram		
B51	6,281,042	B1	Ahn et al.		
B52	6,291,858	B1	Ma et al.		
B53	6,307,257	B1	Huan et al.		
B54	6,314,013	B1	Ahn et al.		
B55	6,322,903	B1	Siniaguine et al.		
B56	6,337,521	B1	Masuda		
B57	6,353,265	B1	Michii		
B58	6,355,501	B1	Fung et al.		
B59	6,197,641	B1	Hergenrother et al.		

FOREIGN PATENT DOCUMENTS						
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		Office ³	Number ⁴			
B60	EPO	0 073 486	A2	Toyama et al.	8-26-1982	
B61	JP	61-222216		Yohehara	10-2-1986	
B62	WO	94/26083		Carson et al.	11-10-1994	
B63	EPO	0 516 866	A1	Bayer et al.	12-9-1992	
B64	EPO	0 644 548	A2	Bertin	9-2-1994	
B65	EPO	0 800 137	A1	Genduso et al.	3-14-1997	
B66	EPO	0 606 653	A1	Harward et al.	7-20-1994	
B67	EPO	0 395 886	A2	Oota et al.	11-7-1990	
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B69	JP	6-22352		Toshiba		
B70	EPO	0 387 834	A2	Wada	9-14-1990	

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Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/066,376
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				Attorney Docket Number	035905-0118

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ⁶
	B71	ABOU-SAMRA S.J.: "3D CMOS SOI for High Performance Computing", Low Power Electronics and Design Proceedings, 1998.			
	B72	YAMAZAKI K.: "4-Layer 3-D IC Technologies for Parallel Signal Processing", International Electron Devices Meeting Technical Digest, December 9-12, 1990, pgs 25.5.1 - 25.5.4.			
	B73	SCHLAEPPPI H.P.: "nd Core Memories using Multiple Coincidence", IRE Transactions on Electronic Computers, June 1960, pgs 192 - 196.			
	B74	SCHLAEPPPI H.P.: "Session V: Information Storage Techniques", International Solid-State Circuits Conference, February 11, 1960, pgs. 54-55.			
	B75	DE GRAAF C. et al.: "A Novel High-Density, Low-Cost Diode Programmable Read Only Memory," IEDM, beginning at page 189			
	B76	PETER K. NAJI et al.: "A 256kb 3.0V 1T1MTJ Nonvolatile Magnetoresistive RAM," 2001 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC 2001/Session 7/Technology Directions: Advanced Technologies/7.6, February 6, 2001, pp. 122-123 (including enlargement of figures, totaling 9 pages), and associated Visual Supplement, pp. 94-95,4040-405 (enlargements of slides submitted, totaling 25 pages)			
	B77	KIM C. HARDEE et al.: "A Fault-Tolerant 30 ns/375 mW 16K x 1 NMOS Static RAM," IEEE Journal of Solid-State Circuits, October 1981, Vol. SC-16, No. 5, pages 435-443			
	B78	TOSHIO WADA et al.: "A 15-ns 1024-Bit Fully Static MOS RAM," IEEE Journal of Solid-State Circuits, October 1978, Vol. SC-13, No. 5, pages 635-639			
	B79	CAMPERI-GINESTET C.: "Vertical Electrical Interconnection of Compound Semiconductor Thin-Film Devices to Underlying Silicon Circuitry", IEEE Photonics Technology Letters, Vol. 4, No. 9, September 1992, pgs. 1003-1006.			
	B80	AKASAKA YOICHI: Three-dimensional Integrated Circuit: Technology and Application Prospect", Microelectronics Journal, Vol. 20, No.s 1-2, 1989, pgs. 105 - 112.			
	B81	SAKAMOTO KAJI: "Architecture des Circuits a Trois Dimension (Architecture of Three Dimensional Devices)", Bulletin of the Electrotechnical Laboratory, ISSN 0366-9092, Vol. 51, No. 1, 1987, pgs 16 - 29.			
	B82	AKASAKA YOICHI: "Three-dimensional IC Trends", "Proceedings of the IEEE, Vol. 74, No. 12, 1986, Pgs. 1703 - 1714.			

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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	B83	CARTER WILLIAM H.: "National Science Foundation (NSF) Forum on Optical Science and Engineering", Proceedings SPIE - The International Society for Optical Engineering, Vol. 2524, July 11 - 12 1995, (Article by N. Joverst titled "Manufacturable Multi-Material Integration Compound Semi-conductor Devices Bonded to Silicon Circuitry".	
	B84	HAYASHI Y.: "A New Three Dimensional IC Fabrication Technology, Stacking Thin Film Dual-CMOS Layers", IEDM, 1991, pgs. 25.6.1 - 25.6.4.	
	B85	REBER M.: "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic", IEEE, 1996, pgs. 121-124.	
	B86	STERN JON M.: "Design and Evaluation of an Epoxy Three-dimensional Multichip Module, IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19, No. 1, February 1996, pgs 188-194.	
	B87	BERTIN CLAUDE L.: "Evaluation of a Three-dimensional Memory Cube System", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 16, No. 8, December 1993, pgs. 1006 - 1011.	
	B88	WATANABE HIDEHIRO: "Stacked Capacitor Cells for High-density Dynamic RAMs", IEDM, 1988, pgs. 600 - 603.	
	B89	WEB PAGE: "Stacked Memory Modules", IBM Technical Disclosure Bulletin, Vol. 38, No. 5, 1995.	
	B90	THAKUR SHASHIDHAR: "An Optimal Layer Assignment Algorithm for Minimizing Crosstalk for Three VHV Channel Routing", IEDM, 1995, pgs. 207 - 210.	
	B91	TERRIL ROB: "3D Packaging Technology Overview and Mass Memory Applications", IEDM, 1996, pgs. 347 - 355.	
	B92	INOUE Y.: "A Three-Dimensional Static RAM", IEEE Electron Device Letters, Vol. 7, No. 5, May 1986, pgs. 327 - 329.	
	B93	REBER M.: "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic", IEDM, 1996, pgs. 121 - 124.	
	B94	KUROKAWA TAKAKAZU: "3-D VLSI Technology in Japan and an Example: A Syndrome Decoder for Double Error Correction", FGCS - Future, Generation, Computer, Systems", Vol. 4, No. 2, 1988, pgs. 145-155, Amsterdam, The Netherlands.	

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	B95	MAKINIAK DAVID: "Vertical Integration of Silicon Allows Packaging of Extremely Dense System Memory In Tiny Volumes: Memory-chip Stacks Send Density Skyward", Electronic Design, No. 17, August 22, 1994, pgs. 69-75, Cleveland Ohio.	
	B96	YAMAZAKI K.: "Fabrication Technologies for Dual 4-KBIT Stacked SRAM", IEDM 16.8., 1986, pgs. 435-438.	
	B97	PEIN HOWARD: "Performance of the 3-D PENCIL Flash EPROM Cell an Memory Array", IEEE Transactions on Electron Devices, Vol. 42, No. 11, November 1995, pgs. 1982-1991.	
	B98	Abstract LOMATCH S.: "Multilayered Josephson Junction Logic and Memory Devices", Proceedings of the SPIE-The International Society for Optical Engineering Vol. 2157, pgs. 332-343.	
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	B101	Abstract "Wide Application of Low-Cost Associative Processing Associative Processing Seen", Electronic Engineering Times, August 26, 1996, pg. 43.	
	B102	Abstract "Interconnects & Packaging", Electronic Engineering Times, November 27, 1995, pg. 43.	
	B103	Abstract "Closing in on Gigabit DRAMs", Electronic Engineering Times, November 27, 1995, pg. 35.	
	B104	Abstract "Module Pact Pairs Cubic Memory with VisionTek", Semiconductor Industry & Business Survey, Vol. 17, No. 15, October 23, 1995.	
	B105	Abstract "Layers of BST Materials Push Toward 1Gbit DRAM", Electronics Times, October 19, 1995.	
	B106	Abstract "Technologies Will Pursue Higher DRAM Densities", Electronic News (1991), December 4, 1994, pg. 12.	

Examiner
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	B107	Abstract "Looking Diverse Storage", Electronic Engineering Times, October 31, 1994, pg. 44.	
	B108	Abstract "Special Report: Memory Market Startups Cubic Memory: 3D Space Savers", Semiconductor Industry & Business Survey, Vol. 16, No. 13, September 12, 1994.	
	B109	Abstract "Technique Boosts 3D Memory Density", Electronic Engineering Times, August 29, 1994, pg. 16.	
	B110	Abstract "Memory Packs Poised 3D Use", Electronic Engineering Times, December 7, 1992, pg. 82.	
	B111	Abstract "MCMs Hit the Road", Electronic Engineering Times, June 15, 1992, pg. 45.	
	B112	Abstract "IEDM Ponders the 'Gigachip' Era", Electronic Engineering Times, January 20, 1992, pg. 33.	
	B113	Abstract "Tech Watch: 1-Gbit DRAM in Sight", Electronic World News, December 16, 1991, pg. 20.	
	B114	Abstract "MCMs Meld into Systems", Electronic Engineering Times, July 22, 1991, pg. 35.	
	B115	Abstract "Systems EEs See Future in 3D", Electronic Engineering Times, September 24, 1990, pg. 37.	
	B116	Patent Application, NISHIURA, US 2001/00054759 A1.	
	B117	Patent Application, FURUSAWA, US 2002/0024146 A1.	
	B118	Patent Application, FUJIMOTO et al, US 2002/0027275 A1.	

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				Attorney Docket Number	035905-0118

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

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	B119	Patent Application, AKRAM, US 2002/0030262 A1.	
	B120	Patent Application, AKRAM, US 2002/0030263 A1.	
	B121	Patent Application, LEEDY, US 2001/0033030 A1.	
	B122	Chan et al. "Three Dimensional CMOS integrated Circuits on Large Grain Polysilicon Films" EEE, Hong Kong University of Science and Technology 2000 IEEE	

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